PATENT
Atty. Docket No.: ALSC-00300

#7 A 7/31/01 V Short

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Shrivastava

Serial No. 09/315,599

Filed: 05/20/99

For: **METHOD AND APPARATUS FOR INTEGRATING FLASH EEPROM AND SRAM CELLS ON A COMMON SUBSTRATE**

Group Art Unit: 2814
Examiner: Ha, N.

RESPONSE TO OFFICE ACTION MAILED ON Apr. 25, 2001

260 Sheridan Ave., Suite 420
Palo Alto, CA 94306
(650) 833-0160

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

REMARKS

Applicants respectfully request further examination and reconsideration in view of the comments set forth fully below. Within the Office Action, all of the Claims 1-10 were rejected. Claims 1-10 still remain pending.

Rejections Under 35 U.S.C. § 103

Claims 1-10 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,605,853 to Yoo et al. (hereinafter "Yoo") in view of U.S. Patent No. 5,679,599 to Mehta (hereinafter "Mehta"). The Applicant respectfully disagrees with this rejection.

Yoo teaches a method of forming a SRAM, a floating gate memory, and a logic device on the same integrated circuit. Specifically, Yoo teaches a method of forming simultaneously a SRAM and an EEPROM on the same integrated circuit, using a LOCOS isolation process. [Yoo, col 3, lines 51-55] Yoo teaches a method of forming a plurality of field isolation regions using a LOCOS isolation process. [Yoo, col 3, line 55-60] Yoo does not teach or suggest that a SRAM and an EEPROM can be formed on the same IC, using a non-LOCOS isolation process, such as a shallow trench isolation (STI) process. Nor does Yoo teach or suggest that a SRAM and an

EEPROM can be formed on the same IC, using a combination of a LOCOS and STI isolation process.

Mehta teaches a device and method for isolating regions of the circuit device in a semiconductor substrate. The method comprises the following steps: forming a first insulation region and a second insulation region; etching a trench in the first insulation region, the trench extending below the surface of the substrate; filling the first isolation region with an isolation material and removing a portion of the isolation material such that the trench isolation material fills the trench and has a surface level with the surface of the substrate; and thermally growing a field oxide in the first and second isolation regions. [Mehta, Abstract and col. 4, line 46- col. 6, line 49] Mehta teaches a method of combining a LOCOS isolation process and structure, with a trench isolation process and structure, wherein a field oxide is grown which simultaneously forms a portion of the LOCOS region and trench isolation structure. [Mehta, col 4, line 47-51, emphasis added] However, Mehta does not teach or suggest a method of combining a LOCOS isolation process and structure, with a trench isolation process and structure, wherein a field oxide is grown which *independently* or *sequentially* forms a portion of the LOCOS region and trench isolation structure. Furthermore, Mehta does not teach a separation technique for growing flash EPROM and SRAM on a common substrate.

In contrast to the teachings of Mehta, Yoo and their combination, the present invention teaches a system for and a method of *independently* or *sequentially* integrating SRAM cells and flash EPROM cells onto a single silicon substrate. Notwithstanding, neither Mehta, Yoo nor their combination teaches or suggests forming a SRAM and an EEPROM on a single substrate using a combination of a LOCOS and STI isolation process. In column 2, line 18-26, Yoo states the following:

> It may be also desirable to form more than one type of memory structure on the same IC, such as an SRAM in conjunction with an EEPROM (Electrically Eraseable Programmable Read Only Memory), as well as logic devices. However, such an IC is difficult to fabricate due to the difference in the typical processes for forming memory and logic and for forming significantly different memory devices.

This statement suggests that Yoo's invention is directed to a method of combining a SRAM and an EEPROM on the same IC, when the same LOCOS isolation process is used on all the regions of the substrate. By this statement, Yoo further concedes that his method does not solve the difficulty of fabricating a SRAM and an EEPROM on the same substrate. Rather, Yoo suggests that an alternative to finding a method of combining two methods would be to improve the current LOCOS isolation method so as to be used on both the SRAM and EEPROM.

Therefore, it would not have been obvious to one skillful in the art, that Yoo could have been combined with Mehta to disclose the current invention. Further, Yoo appears to be teaching away from using multiple different isolation processes on a single IC. Yoo acknowledges the inherent difficulty of applying multiple different isolation processes on an IC, and does not suggest or teach a method of applying a LOCOS and STI isolation process on the same substrate, therefore it would not have been obvious to one skillful in the art from the teachings of Yoo, that a LOCOS and STI isolation process could have been used to form a SRAM and an EEPROM on a common substrate.

The independent Claim 1 is directed to a semiconductor device which comprises a common substrate, a SRAM device implemented on the common substrate and isolated by a first isolation technique and a flash EPROM implemented on the common substrate and isolated by a second isolation technique. As described above, neither Mehta, Yoo nor their combination, teach or suggest a SRAM device implemented on the common substrate and isolated by a first isolation technique and a flash EPROM implemented on the common substrate and isolated by a second isolation technique. For at least these reasons, the independent Claim 1 is allowable over the teachings of Mehta, Yoo and their combination.

Claims 2, 3, and 4 are dependent on the independent Claim 1. As discussed above, the independent Claim 1 is allowable over the teachings of Mehta, Yoo and their combination. Accordingly, the dependent Claims 2, 3, and 4 are allowable as being dependent on an allowable base claim.

The independent Claim 5 is directed to a system for allowing different types of isolation techniques during fabrication of a semiconductor device. The system of Claim 5 comprises a common substrate having a first portion on which a first isolation technique is implemented during processing and a second portion on which a second isolation technique is implemented during processing. The system of Claim 5 also includes an SRAM device implemented on the first portion of the substrate and a flash EPROM device, implemented on the second portion of the substrate. As discussed above, neither Mehta, Yoo nor their combination teach implementing an SRAM device, isolated by a first isolation technique, on a common substrate with a flash EPROM device, isolated by a second isolation technique. For at least these reasons, the independent Claim 5 is allowable over the teachings of Mehta, Yoo and their combination.

Claims 6, 7, and 8 are all dependent on the independent Claim 5. As discussed above, the independent Claim 5 is allowable over the teachings of Mehta, Yoo and their combination. Accordingly, the dependent Claims 6, 7 and 8 are also allowable as being dependent on an allowable base claim.

The independent Claim 9 is directed to a semiconductor device comprising a common substrate having a first portion on which an STI isolation technique is implemented during processing and a second portion on which a LOCOS isolation technique is implemented during processing. The device of Claim 9 also includes an SRAM device implemented on the first portion of the substrate and a flash EPROM device implemented on the second portion of the substrate. As discussed above, neither Mehta, Yoo nor their combination teach implementing an SRAM device, isolated by an STI technique, on a common substrate with a flash EPROM device, isolated by a LOCOS isolation technique. For at least these reasons, the independent Claim 9 is allowable over the teachings of Mehta, Yoo and their combination.

Claim 10 is dependent on the independent Claim 9. As discussed above, the independent Claim 9 is allowable over the teachings of Mehta, Yoo and their combination. Accordingly, the dependent Claim 10 is also allowable as being dependent on an allowable base claim.

For the reasons given above, applicants respectfully submit that the claims are now in a condition for allowance, and allowance at an early date would be appreciated. Should the Examiner have any questions or comments, they are encouraged to call the undersigned at (650) 833-0160 to discuss the same so that any outstanding issues can be expeditiously resolved.

Respectfully submitted,
HAVERSTOCK & OWENS LLP

Dated: July 17, 2001

By: Jonathan O. Owens
Jonathan O. Owens
Reg. No. 37,902
Attorneys for Applicant(s)

CERTIFICATE OF MAILING (37 CFR § 1.8(a))

I hereby certify that this paper (along with any referred to as being attached or enclosed) is being deposited with the U.S. Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to the: Assistant Commissioner for Patents, Washington D.C. 20231

HAVERSTOCK & OWENS LLP

Dat 7/17/01 By: Arleen O'Brien